UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,804	01/27/2004	Paul A. Ingersoll	SC13113TP	2461

23125 7590 04/20/2005

FREESCALE SEMICONDUCTOR, INC.
LAW DEPARTMENT
7700 WEST PARMER LANE MD:TX32/PL02
AUSTIN, TX 78729

EXAMINER	
KEBEDE, BROOK	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 04/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/765,804	INGERSOLL ET AL.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) *29-38* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 8-28* is/are rejected.

7)☒ Claim(s) *5-7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/27/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicants' election with traverse of the Group I invention, claim(s) 1-27, in the response filed on March 4, 2005, is acknowledged. The traversal is on the ground(s) that "Examiner is contending that the restriction is proper because "forming a plurality of discrete elements" does not include bonding discrete elements. This is incorrect. Forming includes any method by which the plurality of discrete elements can be formed. Hence, forming includes bonding and hence. bonding is not independent and distinct from forming. Thus, Applicants fail to see how a materially different process is used. The example given by the Examiner is not correct and thus the Examiner has failed to show how the product as claimed can be made by a materially different process or how the process as claimed can be used to make a materially different product. Independent claim 29 of Group II does not include the feature of "a plurality of discrete elements over the first interfacial layer." Instead claim 29 includes, "a plurality of discrete elements over the first floating gate." In addition, the search and examination of all claims would not be a serious burden on the Examiner. A search of the device claims would involve searching for any method of forming discrete elements, which are included in the method claims..." This is not found persuasive.

A restriction requirement between one set of product claims and a set of process claims was issued in the Office action mailed on February 15, 2005. "Section 121 [of Title 35 USC] permits a restriction for 'independent and distinct inventions,' which the PTO construes to mean that the sets of claims must be drawn to separately patentable inventions." See *Applied Materials Inc. v. Advanced Semiconductor Materials* 40 USPQ2d 1481, 1492 (Fed. Cir 1996)(Archer, C.J.,

concurring in-part and dissenting in-part). A product and the process of making the product are "two independent, albeit related inventions." See *In re Taylor*, 149 USPQ 615, 617 (CCPA 1966). "When two sets of claims filed in the same application are patentably distinct or represent independent inventions, the examiner is to issue a restriction requirement." See *In re Berg*, 46 USPQ2d 1226, 1233 n.10 (Fed. Cir. 1998).

The examiner, in issuing a restriction requirement, must demonstrate "one way distinctiveness." *Applied Materials Inc.* at 1492. As stated within the restriction requirement, "inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f))." In this application, the examiner restricted the product claims from the process claims on the grounds that "the product as claimed can be made by another and materially different process such as a process wherein the device of Group II can be fabricated by bonding of a plurality of discrete elements over the first interfacial layer instead of forming," and that, as a result, a restriction was necessary. Furthermore, the scope of the claimed invention of instant application is determined in light of the supporting disclosure. However, bonding is not one of the scope that is disclosed in the claimed invention.

In addition to one way distinctiveness, the examiner must show "why it would be a burden to examine both sets of claims." *Applied Materials Inc.* at 1492. "A serious burden on the examiner may be *prima facie* shown if the examiner shows by appropriate explanation either separate classification, separate status in the art, or a different field of search." MPEP 803. An explanation was provided in the restriction requirement. Specifically, in addition to being

distinct, the examiner indicated that restriction is proper because the product claims and the process claims "have acquired a separate status in the art."

The criteria of distinctness and burdensomeness have been met, as demonstrated hereinabove. Accordingly, the restriction requirement in this application is still deemed proper and is therefore **made FINAL**.

2. Accordingly, claims 29-38 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention, the requirement having been traversed in the response filed on March 4, 2005.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 12-15, 17, 22-24, 27 and 28 rejected under 35 U.S.C. 102(e) as being anticipated by Lojek (US/6,690,059).

Re claim 1, Lojek discloses a method for forming a semiconductor structure, comprising: providing a semiconductor substrate (not labeled) (see Figs. 1-3 , 8 and 9); forming a first tunnel dielectric (17) overlying the semiconductor substrate (not labeled); forming a first floating gate

(19) overlying the first tunnel dielectric (17); depositing a plurality of pre-formed discrete elements (i.e., nano-crystals) (23) over the first floating gate (19); forming a control dielectric (25) overlying the plurality of pre-formed discrete elements (23); and forming a control gate (27) overlying the control dielectric (25) (see Figs. 1-4, 8 and 9 and related text in Col. 2, line 45 – Col. 3, line 67).

Re claim 12, as applied to claim 1 above, Lojek discloses all the claimed limitations including the limitation wherein the plurality of pre-formed discrete elements are further characterized as pre-fabricated discrete elements (see Figs. 1-3, 8 and 9).

Re claim 13, as applied to claim 1 above, Lojek discloses all the claimed limitations including the limitation wherein the plurality of pre-formed discrete elements comprise nanocrystals (see Figs. 1-3, 8 and 9).

Re claim 14, as applied to claim 1 above, Lojek discloses all the claimed limitations including the limitation wherein the plurality of pre-formed discrete elements comprise discrete storage elements (see Figs. 1-3, 8 and 9).

Re claim 15, as applied to claim 1 above, Lojek discloses all the claimed limitations including the limitation wherein each of the plurality of pre-formed discrete elements comprise a substantially conductive material (see Figs. 1-3, 8 and 9).

Re claim 17, Lojek discloses a method for forming a semiconductor structure, comprising: providing a semiconductor substrate (not labeled); forming a first tunnel dielectric overlying (17 or 107) the semiconductor substrate (not labeled); forming a first floating gate (19 or 109) overlying the first tunnel dielectric (17 or 107); forming a first interfacial layer (see Figs. 1 and 8) overlying the first floating gate (19 or 109); forming a plurality of discrete elements (23

or 113) over the first interfacial layer (see Figs. 1 and 8); forming a control dielectric (25 or 115, 117, 117) overlying the plurality of discrete elements (23 or 113); and forming a control gate (27or 121) overlying the control dielectric (see Figs. 1-3, 8 and 9).

Re claim 22, as applied to claim 17 above, Lojek discloses all the claimed limitations including the limitation wherein the plurality of discrete elements comprise nanocrystals (see Figs. 1-3, 8 and 9).

Re claim 23, as applied to claim 17 above, Lojek discloses all the claimed limitations including the limitation wherein the plurality of discrete elements comprise discrete storage elements (see Figs. 1-3, 8 and 9).

Re claim 24, as applied to claim 17 above, Lojek discloses all the claimed limitations including the limitation wherein each of the plurality of discrete elements comprise a substantially conductive material (see Figs. 1-3, 8 and 9).

Re claim 27, as applied to claim 17 above, Lojek discloses all the claimed limitations including the limitation wherein forming a first interfacial layer overlying the first floating gate comprises forming an oxide layer overlying the first floating gate (see Figs. 1-3, 8 and 9).

Re claim 28, as applied to claim 17 above, Lojek discloses all the claimed limitations including the limitation wherein forming a first interfacial layer overlying the first floating gate comprises forming a metal layer overlying the first floating gate (see Figs. 1-3, 8 and 9).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 16 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over (US/6,690,059).

Re claim 16, as applied to claim 1 in Paragraph 5 above. Lojek et al. disclose all the claimed limitation including depositing the plurality of pre-formed discrete elements in predetermined distance.

However, the claimed spacing distance of the discrete elements can be optimized by one having ordinary skill in the art in order to achieve the desire device performance and size.

Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are

otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966). See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed distance between each of discrete elements or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

Re claim 26, as applied to claim 17 in Paragraph 5 above. Lojek et al. disclose all the claimed limitation including depositing the plurality of pre-formed discrete elements in predetermined distance.

However, the claimed spacing distance of the discrete elements can be optimized by one having ordinary skill in the art in order to achieve the desire device performance and size.

Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are

otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966). See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed distance between each of discrete elements or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

8. Claims 2-4, 8, 10 and 18 - 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lojek (US/6,690,059), in Paragraph 5 above, in view of Kim et al. (US/6,844,231).

Re claim 2, as applied to claim 1 in Paragraph 5 above, Lojek discloses all the claimed limitations including forming an isolation trench (not labeled) in the semiconductor substrate (not labeled); filling the isolation trench with a trench fill material (see Figs. 1-4, 8 and 9)

However, Lojek does not specifically disclose forming a second tunnel dielectric overlying the semiconductor substrate; and forming a second floating gate overlying the second tunnel dielectric, wherein the trench fill material is between the first floating gate and the second floating (i.e., the second transistor region between the STI).

Kim et al. disclose forming a second tunnel dielectric (28) overlying the semiconductor substrate (10); and forming a second floating gate (32) overlying the second tunnel dielectric

(28), a trench fill material I24) is between the first floating gate and the second floating (see Fig. 1K) in order to form number of transistors region on a single substrate.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Lojek reference with forming a second tunnel dielectric overlying the semiconductor substrate; and forming a second floating gate overlying the second tunnel dielectric, wherein the trench fill material is between the first floating gate and the second floating as taught by Kim et al. in order to form number of transistors region on a single substrate.

Re claim 3, as applied to claim 2 above, Lojek and Kin et al. in combination disclose all the claimed limitations including wherein depositing the plurality of pre-formed discrete elements over the first floating gate further comprises depositing the plurality of pre-formed discrete elements over the trench fill material and the second floating gate (not shown) (see Lojek Figs. 1 and 8).

Re claim 4, as applied to claim 3 above, Lojek and Kin et al. in combination disclose all the claimed limitations including the limitation wherein forming the control dielectric is performed such that the control (27) dielectric overlies the plurality of pre-formed discrete elements overlying the first floating gate (19), the trench fill material (not labeled), and the second floating gate (not shown) (see Lojek Figs. 1 and 8).

Re claim 8, as applied to claim 1 in Paragraph 5 above, Lojek discloses all the claimed limitation including forming floating gate comprises conductive material.

However, Lojek dose not specifically disclose polysilicon used as floating gate.

Kim et al. disclose the use of polysilicon material as floating gate (32), as well-known in the art, because polysilicon can easily deposited with known process on the substrate and implanted and patterned to be used as gate.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Lojek reference with polysilicon floating gate as taught by Kim et al. because polysilicon can easily deposited with known process on the substrate and implanted and patterned to be used as gate.

Re claim 10, as applied to claim 1 in Paragraph 5 above, Lojek et al. disclose all the claimed limitations including the limitation wherein forming the control dielectric comprises forming an oxide layer (115) overlying the plurality of pre-formed discrete elements (113) (see Fig. 8) and forming a charge trap layer (117) overlying the oxide layer (115) (see Lojek Figs. 8 and 9).

However, Lojek does not specifically disclose the charge trap layer **117** being a nitride layer.

Kim et al. disclose a charge tap layer for nitride layer as ONO structure (34) (see Fig. 1L and Col. 5, lines 60-65) in order to form the dielectric stack between the floating gate and the control gate.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Lojek reference nitride layer over the oxide layer as taught by Kim et al. in order to form the dielectric stack between the floating gate and the control gate.

Re claim 18, as applied to claim 17 in Paragraph 5 above, Lojek discloses all the claimed limitations including forming an isolation trench (not labeled) in the semiconductor substrate (not labeled) ; filling the isolation trench with a trench fill material (see Figs. 1-4, 8 and 9)

However, Lojek does not specifically disclose forming a second tunnel dielectric overlying the semiconductor substrate; and forming a second floating gate overlying the second tunnel dielectric, wherein the trench fill material is between the first floating gate and the second floating (i.e., the second transistor region between the STI).

Kim et al. disclose forming a second tunnel dielectric (28) overlying the semiconductor substrate (10); and forming a second floating gate (32) overlying the second tunnel dielectric (28), a trench fill material I24) is between the first floating gate and the second floating (see Fig. 1K) in order to form number of transistors region on a single substrate.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Lojek reference with forming a second tunnel dielectric overlying the semiconductor substrate; and forming a second floating gate overlying the second tunnel dielectric, wherein the trench fill material is between the first floating gate and the second floating as taught by Kim et al. in order to form number of transistors region on a single substrate.

Re claim 19, as applied to claim 18 above, Lojek and Kim et al. in combination disclose all the claimed limitations including the limitation wherein forming the plurality of discrete elements over the first interfacial layer further comprises depositing the plurality of pre-formed discrete elements over the trench fill material and the second interfacial layer.

Re claim 20, as applied to claim 18 above, Lojek and Kim et al. in combination disclose all the claimed limitations including the limitation wherein forming the control dielectric is performed such that the control dielectric overlies the plurality of discrete elements overlying the first floating gate, the trench fill material, and the second floating gate.

Re claim 21, as applied to claim 17 in Paragraph 5 above, Lojek discloses all the claimed limitation including forming floating gate comprises conductive material.

However, Lojek dose not specifically disclose the floating gate comprises one of polysilicon and metal.

Kim et al. disclose the use of polysilicon material as floating gate (32), as well-known in the art, because polysilicon can easily deposited with known process on the substrate and implanted and patterned to be used as gate.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Lojek reference with polysilicon floating gate as taught by Kim et al. because polysilicon can easily deposited with known process on the substrate and implanted and patterned to be used as gate.

9. Claims 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lojek (US/6,690,059), as applied in Paragraph 5 above, in view of Forbes (US/2003/0234420).

Re claim 9, as applied to claim 1 in Paragraph 5 above, Lojek disclose all the calimed limitation including forming of the floating gate.

However, Lojek does not specifically disclose the floating gate comprising metal.

Forbes discloses forming a metal floating gate (see Page 7 and Paragraph [0063]). As Forbes discloses, the metal floating gate has work function higher than the conventional

polysilicon floating gate and as result it the tunneling current and can be lowered and the device will have longer retention times. The method of claim 1, wherein the first floating gate comprises metal.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Lojek reference with a metal floating gate as taught by Forbes in order to lower the tunneling current which resulted a longer retention time of the device.

10. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lojek (US/6,690,059), as applied in Paragraph 5 above, in view of Arai et al. (US/6,878,985).

Re claim 11, as applied to claim 1in Paragraph 5 above, Lojek discloses all the claimed limitation including the limitations forming a dielectric stack overlaying the discreet elements between the floating gate and the control gate. However, Lojek does not specifically disclose forming of high dielectric constant dielectric layer between the floating gate and the control gate.

Ari et al. disclose forming of a high-K dielectric layer between the floating gate and the control gate (see Col. 7, lines 10-23). Ari et al. also suggest that "the gate insulating layer can be made of a high-dielectric-constant material, and the thickness of the gate insulating layer can be decreased. This makes it possible to increase the capacitance between the floating gate electrode and control gate electrode, and achieve high integration and a low write potential at the same time."

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Lojek reference with high-K inter-dielectric insulating layer between the floating gate and the control gate as taught by Ari et al. in

order the lower the thickness of the dielectric layer and a same time increase the dielectric constant to achieve high integration and a low write potential at the same time.

11. Claims 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lojek (US/6,690,059), as applied in Paragraph 5 above, in view of Batra et al. (US/2003/0235064).

Re claim 5, as applied to claim 17 in Paragraph 5 above, Lojek discloses all the claimed limitations including forming plurality of discrete elements over the first interfacial layer.

However, Lojek does not specifically disclose forming of the plurality of discrete elements using a process selected from the group consisting of low pressure chemical vapor deposition (LPCVD), physical vapor deposition (PVD), and atomic layer deposition (ALD).

Batra et al. disclose forming plurality of discrete elements over the first interfacial layer using a process selected from the group consisting of low pressure chemical vapor deposition (LPCVD), physical vapor deposition (PVD), and atomic layer deposition (ALD) (see Page 2, Paragraph [0021]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Lojek reference forming plurality of discrete elements over the first interfacial layer using a process selected from the group consisting of low pressure chemical vapor deposition (LPCVD), physical vapor deposition (PVD), and atomic layer deposition (ALD) as taught by Batra et al. in order to deposit plurality of discrete elements over the first interfacial layer and from nanocrystals.

Allowable Subject Matter

12. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. Claim 6 is also objected as being dependent of the objected dependent claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. Claim 7 is also objected as being dependent of the objected dependent claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure Choi et al. (US/6,656,792) and Yoshii et al. (US/6,740,928) also disclose similar inventive subject matter.

Correspondence

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brook Kebede

Brook Kebede
Examiner
Art Unit 2823

BK
April 17, 2005